SPECIFICATION
FOR
APPROVAL

( ) Preliminary Specification
(●) Final Specification

Title	42.0” WUXGA TFT LCD

BUYER	General
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LC420WUB
SUFFIX	SCA1

*When you obtain standard approval,
please use the above model name without suffix
* **RoHS will be verified by 1/28**

APPROVED BY	SIGNATURE DATE
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/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE DATE
S. J LEE / Team Leader	
REVIEWED BY	
S. J LEE / Project Leader	
PREPARED BY	
S. M Lee / Engineer	

TV Products Development Dept.
LG Display LCD Co., Ltd

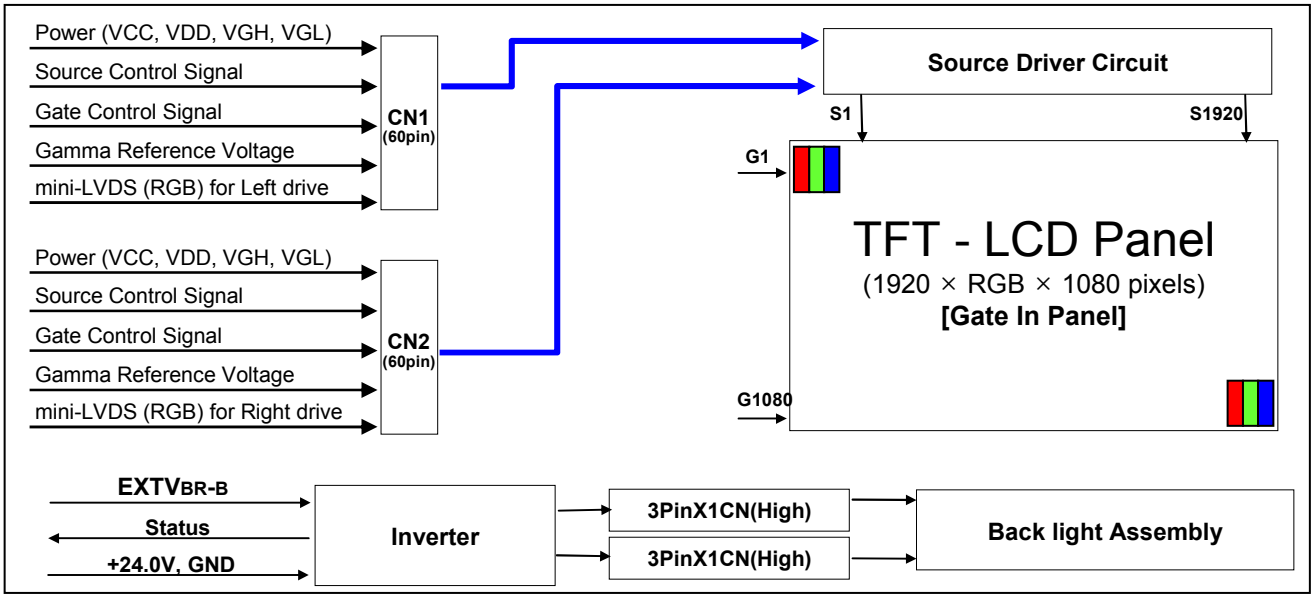
CONTENTS

RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.0	Sep. 1 .2009	-	Preliminary Specification (First Draft)
0.1	Oct. 21 .2009	6	Change Circuit Value
1.0	Jan. 11 .2010	-	Final CAS
1.1	Feb. 22 .2010		

1. General Description

The LC420WUB is a Color Active Matrix Liquid Crystal Display with an integral External Electrode Fluorescent Lamp(EEFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 42.02 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	42.02 inches(1067.31mm) diagonal
Outline Dimension	983.0(H) x 576.0 (V) x 52.0 mm(D) (Typ.)
Pixel Pitch	0.4845 mm x 0.4845 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors
Drive IC Data Interface	Source D-IC : 8-bit mini-LVDS, gamma reference voltage, and control signals Gate D-IC : Gate In Panel
Luminance, White	500 cd/m^2 (Center 1point ,Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total 149 W (Typ.) (Logic=9.0 W with T-CON , Backlight=140W @ with Inverter)
Weight	9.1 Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%)

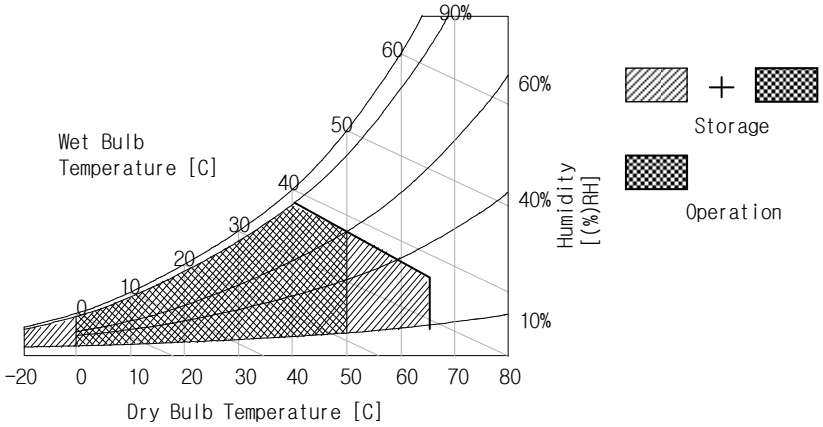
2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Note
			Min	Max		
Inverter Power Input Voltage		V_{BL}	-0.3	+27.0	V_{DC}	
Inverter Control Voltage	ON/OFF	V_{OFF} / V_{ON}	-0.3	+5.5	V_{DC}	
	Brightness	V_{BR}	0.0	+5.0	V_{DC}	
Logic Power Voltage		VCC	-0.5	+4.0	V_{DC}	
Gate High Voltage		VGH	+18.0	+30.0	V_{DC}	1
Gate Low Voltage		VGL	-8.0	-4.0	V_{DC}	
Source D-IC Analog Voltage		VDD	-0.3	+18.0	V_{DC}	
Gamma Ref. Voltage (Upper)		VGMH	½VDD-0.5	VDD+0.5	V_{DC}	
Gamma Ref. Voltage (Low)		VGML	-0.3	½ VDD+0.5	V_{DC}	
Panel Front Temperature		T_{SUR}	-	+68	°C	4
Operating Temperature		T_{OP}	0	+50	°C	2,3
Storage Temperature		T_{ST}	-20	+60	°C	
Operating Ambient Humidity		H_{OP}	10	90	%RH	
Storage Humidity		H_{ST}	10	90	%RH	

Note: 1. Ambient temperature condition (Ta = 25 ± 2 °C)
2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 °C and no condensation of water.
3. Gravity mura can be guaranteed below 40℃ condition.
4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 ℃ with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 ℃. The range of operating temperature may degrade in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and GIP.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	VDC	
Logic High Level Input Voltage	VIH		2.7		VCC	VDC	
Logic Low Level Input Voltage	VIL		0		0.6	VDC	
Source D-IC Analog Voltage	VDD	-	Typ – 500mV	16.25	Typ + 500mV	VDC	
Half Source D-IC Analog Voltage	H_VDD	-	7.9	8.00	8.1	VDC	
Gamma Reference Voltage	V_{GMH}	(GMA1 ~ GMA9)	½*VDD		VDD-0.2		
	V_{GML}	(GMA10 ~ GMA18)	0.2		½*VDD		
Common Voltage	Vcom	-	6.65	6.95	7.25	V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC ≤3.6V			312	MHz	
mini-LVDS input Voltage (Center)	VIB	Mini-LVDS Clock and Data	0.7 + (VID/2)		(VCC-1.2) – VID / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔVIB				0.8	V	
mini-LVDS differential Voltage range	VID		150		800	mV	
mini-LVDS differential Voltage range Dip	ΔVID		25		800	mV	
Gate High Voltage	VGH		**Typ.-1.0V**	**27.69 @ 25℃ 29.15 @ 0℃**	**Typ.+1.0V**	VDC	
Gate Low Voltage	VGL		**Typ – 370mV**	**-5.3**	**Typ + 370mV**	VDC	
GIP Bi-Scan Voltage	VGI_P VGI_N	-	VGL	-	VGH	VDC	
GIP Refresh Voltage	VGH even/odd	-	VGL	-	VGH	V	
GIP Start Pulse Voltage	VST	-	VGL	-	VGH	V	
GIP Operating Clock	GCLK	-	VGL	-	VGH	V	
Total Power Current	ILCD	-	525	750	975	mA	2
Total Power Consumption	PLCD	-		9.0		Watt	2

Note: 1. The specified current and power consumption are under the VLCD=12V., 25 ± 2°C, f_V=120Hz condition whereas mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The above spec is based on the basic model.
3. All of the typical gate voltage should be controlled within 1% voltage level
4. Ripple voltage level is recommended under 10%
5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
6. Logic level Input Signal : SOE, POL, GSP, H_CONV, OPT_N
7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10

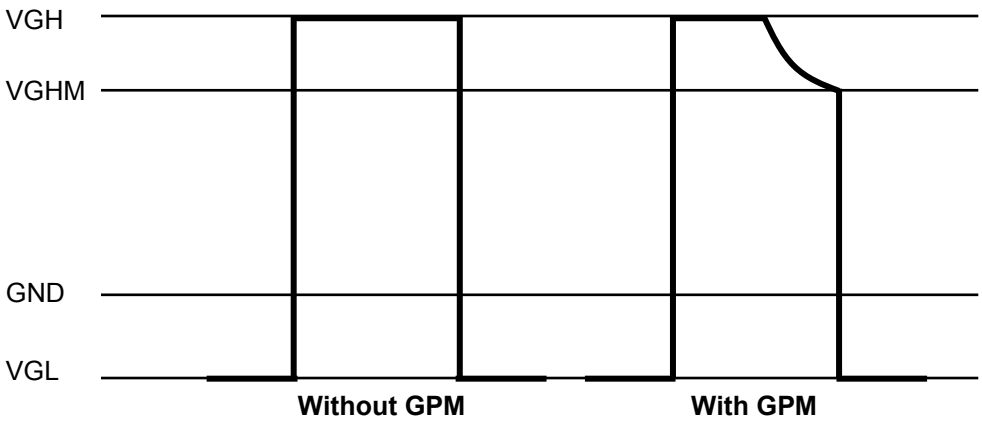


FIG. 1 Gate Output Wave form without GPM and with GPM

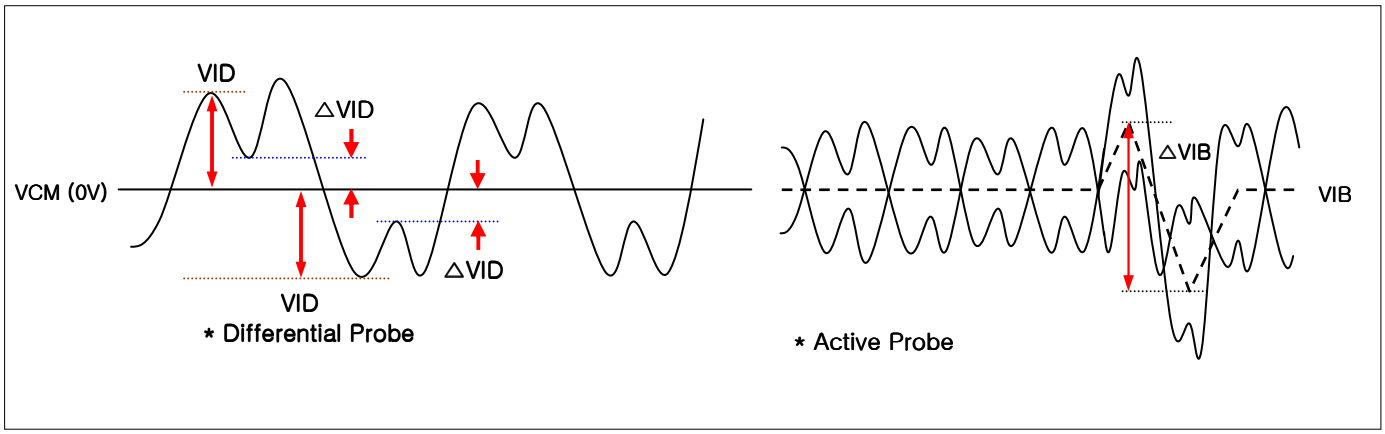


FIG. 2 Description of VID, ΔVIB, ΔVID

* Source PCB

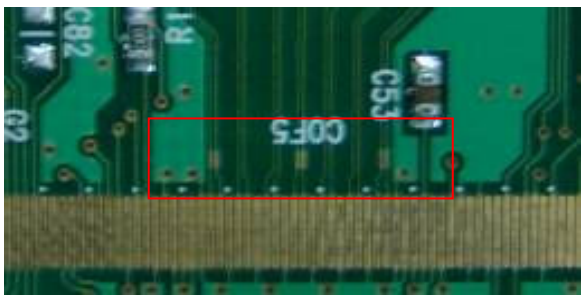


FIG. 3 Measure point

Table 3. ELECTRICAL CHARACTERISTICS (Continue)

Parameter			Symbol	Values			Unit	Note
				Min	Typ	Max		
Inverter :								
Power Supply Input Voltage			V_{BL}	22.8	24.0	25.2	V_{DC}	1
Power Supply Input Current	After Aging		I_{BL_A}	-	5.8	6.7	A	1
	Before Aging		I_{BL_B}	-	7.0	7.5	A	2
Power Supply Input Current (In-Rush)			I_{RUSH}	-	-	11	A	V_{BL} = 22.8V **EXTV**$_{BR-B}$ = 100% 6
Power Consumption			P_{BL}	-	140	160	W	1
Input Voltage for Control System Signals	On/Off	On	V_{ON}	2.5	-	5.0	V_{DC}	
		Off	V_{OFF}	-0.3	0.0	0.8	V_{DC}	
	Brightness Adjust		**EXTV**$_{BR-B}$	20	-	100	%	On Duty 7
	PWM Frequency for NTSC & PAL		PAL		100		Hz	5
			NTSC		120		Hz	5
	Pulse Duty Level (PWM) (Burst mode)		High Level	2.5	-	5.0	V_{DC}	High: Lamp on Low : Lamp off
			Low Level	0.0	-	0.8	V_{DC}	
Lamp:								
Lamp Voltage			V_{OUT}	900	1050	1200	V_{RMS}	**EXTV**$_{BR-B}$ =100% 1
Lamp Current			I_{OUT}	126	136	146	mA_{RMS}	**EXTV**$_{BR-B}$ =100% 1
Discharge Stabilization Time			Ts			3	min	3
Life Time				50,000	60,000		Hrs	4

Note 1. Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 120 minutes at 25±2°C. The specified current and power consumption are under the typical supply Input voltage 24Vand V_{BR} (**EXTV**$_{BR-B}$: 100%), it is total power consumption.

2. Electrical characteristics are determined within 30 minutes at 25±2°C.
   The specified currents are under the typical supply Input voltage 24V.
3. The brightness of the lamp after lighted for 5minutes is defined as 100%.
   Ts is the time required for the brightness of the center of the lamp to be not less than 95% at typical current.
   The screen of LCD module may be partially dark by the time the brightness of lamp is stable after turn on.
4. Specified Values are for a single lamp which is aligned horizontally.
   The life time is determined as the time which luminance of the lamp is 50% compared to that of initial value at the typical lamp current (**EXTV**$_{BR-B}$:100%), on condition of continuous operating at 25± 2°C
5. LGD recommend that the PWM freq. is synchronized with Two times harmonic of Vsync signal of system.
6. The duration of rush current is about 10ms.
7. **EXTV**$_{BR-B}$ is based on input PWM duty of the inverter.

3-2. Interface Connections

This LCD module employs two kinds of interface connection, two 60-pin FFC connector are used for the module electronics and 14/12-pin connectors is used for the integral backlight system.

3-2-1. LCD Module

-LCD Connector (CN1): TF06L-60S-0.5SF (Manufactured by HRS)

Table 4-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description		No	Symbol	Description
1	GND	Ground		31	LLV3 -	Left Mini LVDS Receiver Signal(3-)
2	LTD_OUT	LTD OUTPUT		32	LLV3 +	Left Mini LVDS Receiver Signal(3+)
3	GCLK1	GIP GATE Clock 1		33	LCLK -	Left Mini LVDS Receiver Clock Signal(-)
4	GCLK2	GIP GATE Clock 2		34	LCLK +	Left Mini LVDS Receiver Clock Signal(+)
5	GCLK3	GIP GATE Clock 3		35	LLV2 -	Left Mini LVDS Receiver Signal(2-)
6	GCLK4	GIP GATE Clock 4		36	LLV2 +	Left Mini LVDS Receiver Signal(2+)
7	GCLK5	GIP GATE Clock 5		37	LLV1 -	Left Mini LVDS Receiver Signal(1-)
8	GCLK6	GIP GATE Clock 6		38	LLV1 +	Left Mini LVDS Receiver Signal(1+)
9	VGI_N	VGL		39	LLV0 -	Left Mini LVDS Receiver Signal(0-)
10	VGI_P	VGH		40	LLV0 +	Left Mini LVDS Receiver Signal(0+)
11	VGH_ODD	GIP Panel VDD for Odd GATE TFT		41	GND	Ground
12	VGH_EVEN	GIP Panel VDD for Even GATE TFT		42	SOE	Source Output Enable SIGNAL
13	VGL	GATE Low Voltage		43	POL	Polarity Control Signal
14	VST	VERTICAL START PULSE		44	GSP	GATE Start Pulse
15	GND	Ground		45	H_CONV	"H“ H 2dot Inversion/ "L" H 1dot Inversion
16	VCOM_L_FB	VCOM Left Feed-Back Output		46	OPT_N	“H” Normal Display
17	VCOM_L	VCOM Left Input		47	GND	Ground
18	GND	Ground		48	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)
19	VDD	Driver Power Supply Voltage		49	GMA 16	GAMMA VOLTAGE 16
20	VDD	Driver Power Supply Voltage		50	GMA 15	GAMMA VOLTAGE 15
21	H_VDD	Half Driver Power Supply Voltage		51	GMA 14	GAMMA VOLTAGE 14
22	H_VDD	Half Driver Power Supply Voltage		52	GMA 12	GAMMA VOLTAGE 12
23	GND	Ground		53	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)
24	VCC	Logic Power Supply Voltage		54	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)
25	VCC	Logic Power Supply Voltage		55	GMA 7	GAMMA VOLTAGE 7
26	GND	Ground		56	GMA 5	GAMMA VOLTAGE 5
27	LLV5 -	Left Mini LVDS Receiver Signal(5-)		57	GMA 4	GAMMA VOLTAGE 4
28	LLV5 +	Left Mini LVDS Receiver Signal(5+)		58	GMA 3	GAMMA VOLTAGE 3
29	LLV4 -	Left Mini LVDS Receiver Signal(4-)		59	GMA 1	GAMMA VOLTAGE 1(Output From LCD)
30	LLV4 +	Left Mini LVDS Receiver Signal(4+)		60	GND	Ground

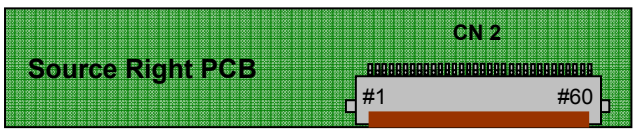
Note : 1. Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.
2. These 'input signal' (OPT_N,H_CONV) should be connected

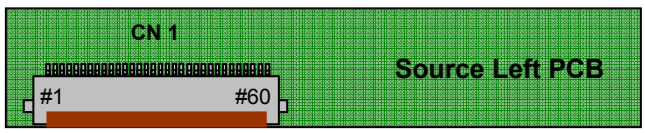
-LCD Connector (CN2): TF06L-60S-0.5SF(Manufactured by HRS)

Table 4-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description		No	Symbol	Description
1	GND	Ground		31	RLV1 -	Right Mini LVDS Receiver Signal(1-)
2	GMA 1	GAMMA VOLTAGE 1 (Output From LCD)		32	RLV1 +	Right Mini LVDS Receiver Signal(1+)
3	GMA 3	GAMMA VOLTAGE 3		33	RLV0 -	Right Mini LVDS Receiver Signal(0-)
4	GMA 4	GAMMA VOLTAGE 4		34	RLV0 +	Right Mini LVDS Receiver Signal(0+)
5	GMA 5	GAMMA VOLTAGE 5		35	GND	Ground
6	GMA 7	GAMMA VOLTAGE 7		36	VCC	Logic Power Supply Voltage
7	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)		37	VCC	Logic Power Supply Voltage
8	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)		38	GND	Ground
9	GMA 12	GAMMA VOLTAGE 12		39	H_VDD	Half Driver Power Supply Voltage
10	GMA 14	GAMMA VOLTAGE 14		40	H_VDD	Half Driver Power Supply Voltage
11	GMA 15	GAMMA VOLTAGE 15		41	VDD	Driver Power Supply Voltage
12	GMA 16	GAMMA VOLTAGE 16		42	VDD	Driver Power Supply Voltage
13	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)		43	GND	Ground
14	GND	Ground		44	VCOM_R	VCOM Right Input
15	OPT_N	“H” Normal Display		45	VCOM_R_FB	VCOM Right Feed-Back Output
16	H_CONV	"H“ H 2dot Inversion/ "L" H 1dot Inversion		46	GND	Ground
17	GSP	GATE Start Pulse		47	VST	VERTICAL START PULSE
18	POL	Polarity Control Signal		48	VGL	GATE Low Voltage
19	SOE	Source Output Enable SIGNAL		49	VGH_EVEN	GIP Panel VDD for Even GATE TFT
20	GND	Ground		50	VGH_ODD	GIP Panel VDD for Odd GATE TFT
21	RLV5 -	Right Mini LVDS Receiver Signal(5-)		51	VGI_P	VGH
22	RLV5 +	Right Mini LVDS Receiver Signal(5+)		52	VGI_N	VGL
23	RLV4 -	Right Mini LVDS Receiver Signal(4-)		53	GCLK6	GIP GATE Clock 6
24	RLV4 +	Right Mini LVDS Receiver Signal(4+)		54	GCLK5	GIP GATE Clock 5
25	RLV3 -	Right Mini LVDS Receiver Signal(3-)		55	GCLK4	GIP GATE Clock 4
26	RLV3 +	Right Mini LVDS Receiver Signal(3+)		56	GCLK3	GIP GATE Clock 3
27	RCLK -	Right Mini LVDS Receiver Clock Signal(-)		57	GCLK2	GIP GATE Clock 2
28	RCLK +	Right Mini LVDS Receiver Clock Signal(+)		58	GCLK1	GIP GATE Clock 1
29	RLV2 -	Right Mini LVDS Receiver Signal(2-)		59	LTD_OUT	LTD OUTPUT
30	RLV2 +	Right Mini LVDS Receiver Signal(2+)		60	GND	Ground

Note : 1.Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.
2. These 'input signal' (OPT_N,H_CONV) should be connected





3-2-2. Backlight Module

[Master]

-Inverter Connector : S14B-PH-SM4(JST)

Mating Connector : PHR-14

[Slave]

-Inverter Connector : S12B-PH-SM3(JST)

-Mating Connector : PHR-12

Table 5. INVERTER CONNECTOR PIN CONFIGULATION

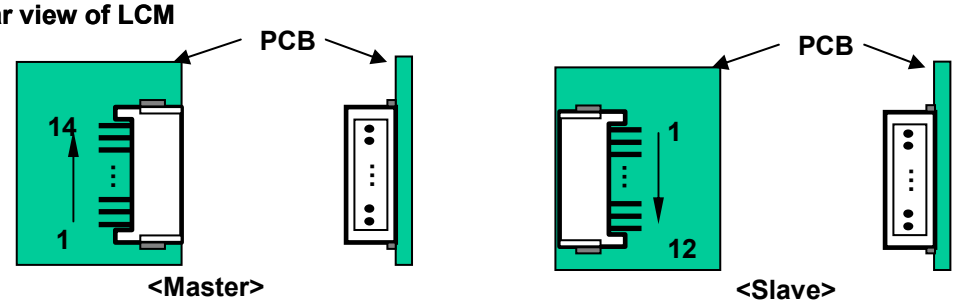
Pin No	Symbol	Description	Master	Slave	Note
1	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
2	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
3	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
4	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
5	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
6	GND	Backlight Ground	GND	GND	
7	GND	Backlight Ground	GND	GND	
8	GND	Backlight Ground	GND	GND	1
9	GND	Backlight Ground	GND	GND	
10	GND	Backlight Ground	GND	GND	
11	NC	No Connection	NC	NC	
12	$V_{ON/OFF}$	Backlight ON/OFF control	$V_{ON/OFF}$	Don't care	3
13	$EXTV_{BR-B}$	External PWM	$EXTV_{BR-B}$	-	3
14	Status	Lamp Status	Status	-	2

Note 1. GND should be connected to the LCD module's metal frame.

2. Normal : Low (under 0.7V) / Abnormal : High (upper 3.0V)
   Please see **Appendix IV-1** for more information.

3. The impedance of pin #12 is over 50[KΩ] & the impedance of Pin #13 is over 100[KΩ].

◆ **Rear view of LCM**



3-3. Signal Timing Specifications

Table 6. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T_1		3.2	3.4		ns	1
Mini Clock pulse low period	T_2		1.6	-	-	ns	
Mini Clock pulse high period	T_3		1.6	-	-	ns	
Mini Data setup time	T_6		0.60	-	-	ns	
Mini Data hold time	T_7		0.60	-	-	ns	
Reset low to SOE rising time	T_8		0	-	-	ns	
SOE to Reset input time	T_9		200	-	-	ns	
Receiver off to SOE timing	T_{10}		10	-	-	CLK cycle	
POL signal to SOE setup time	T_{11}		-5	-	-	ns	
POL signal to SOE hold time	T_{12}		6	-	-	ns	
Reset High Period	T_{13}		3			CLK cycle	
SOE signal GSP setup time	T_{14}		100			ns	
SOE signal GSP Hold time	T_{15}		100			ns	
SOE signal Pulse Width	T_{16}		200			ns	

Note : 1. mini-LVDS timing measure conditions:
: 268 MHz < Clock Frequency <312 MHz , 150mV < VID < 800mV @ 3.0< VCC <3.3
2. Setup time and hold time should be satisfied at the same time

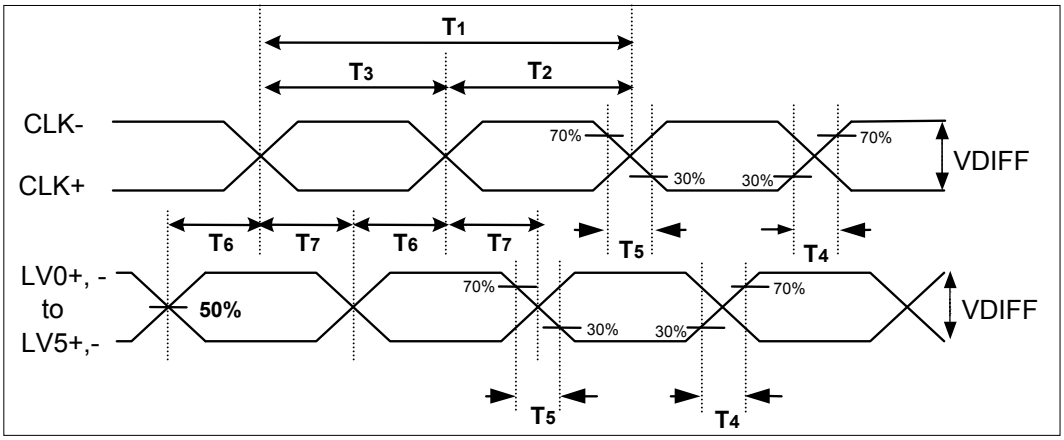


FIG 4. Source D-IC Input Data Latch Timing Waveform

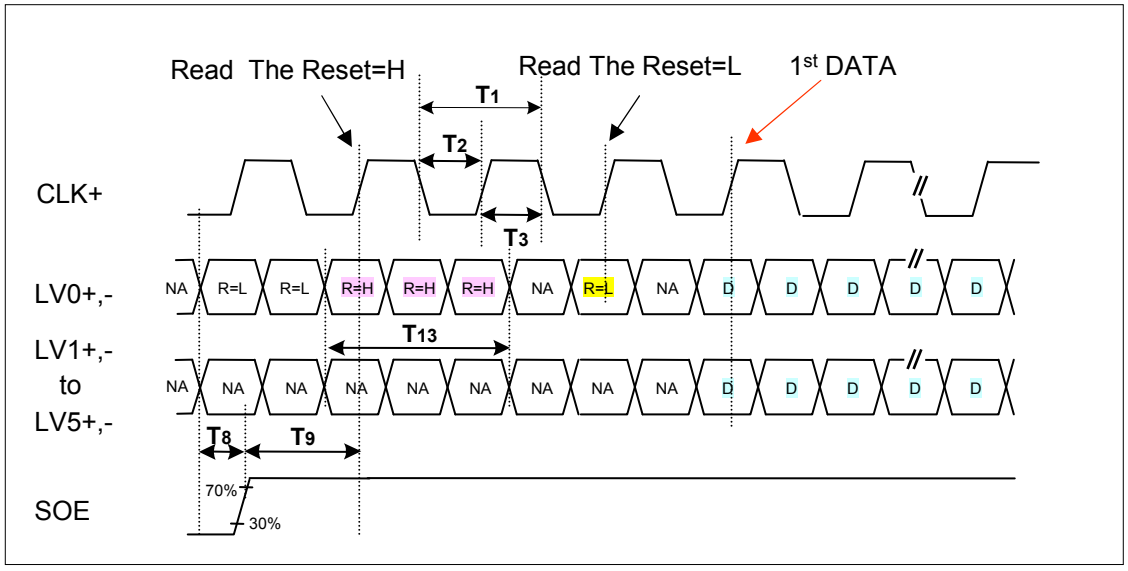


FIG 5-1. Input Data Timing for 1st Source D-IC Chip

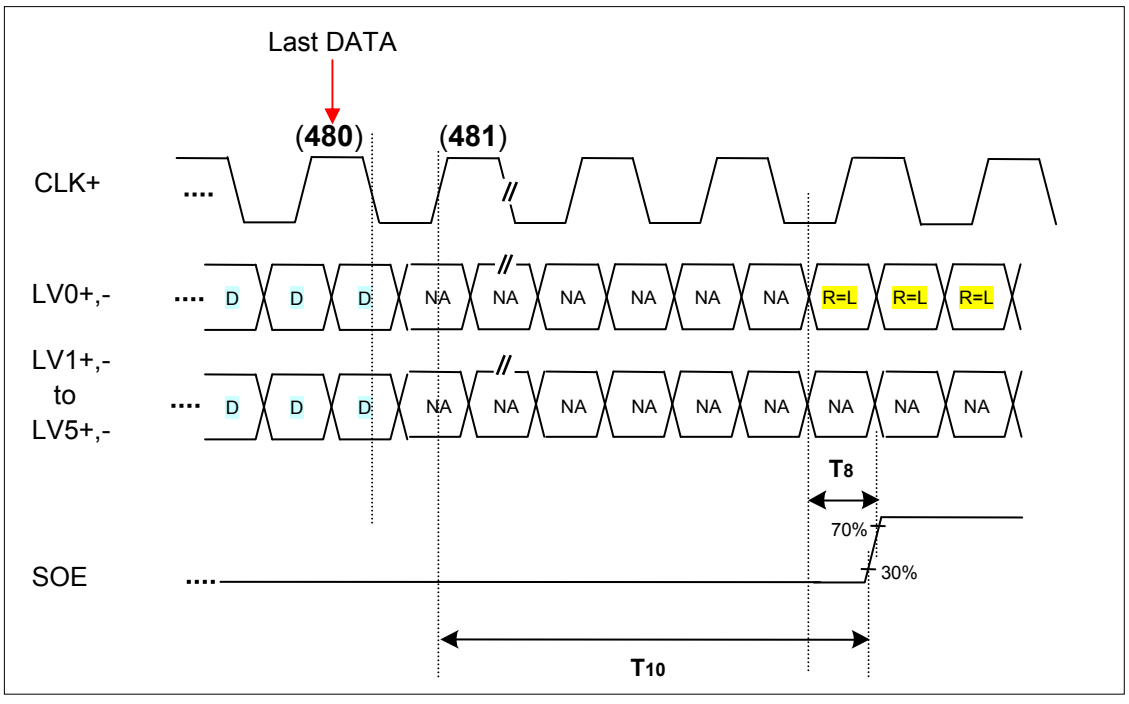


FIG 5-2. Last Data Latch to SOE Timing

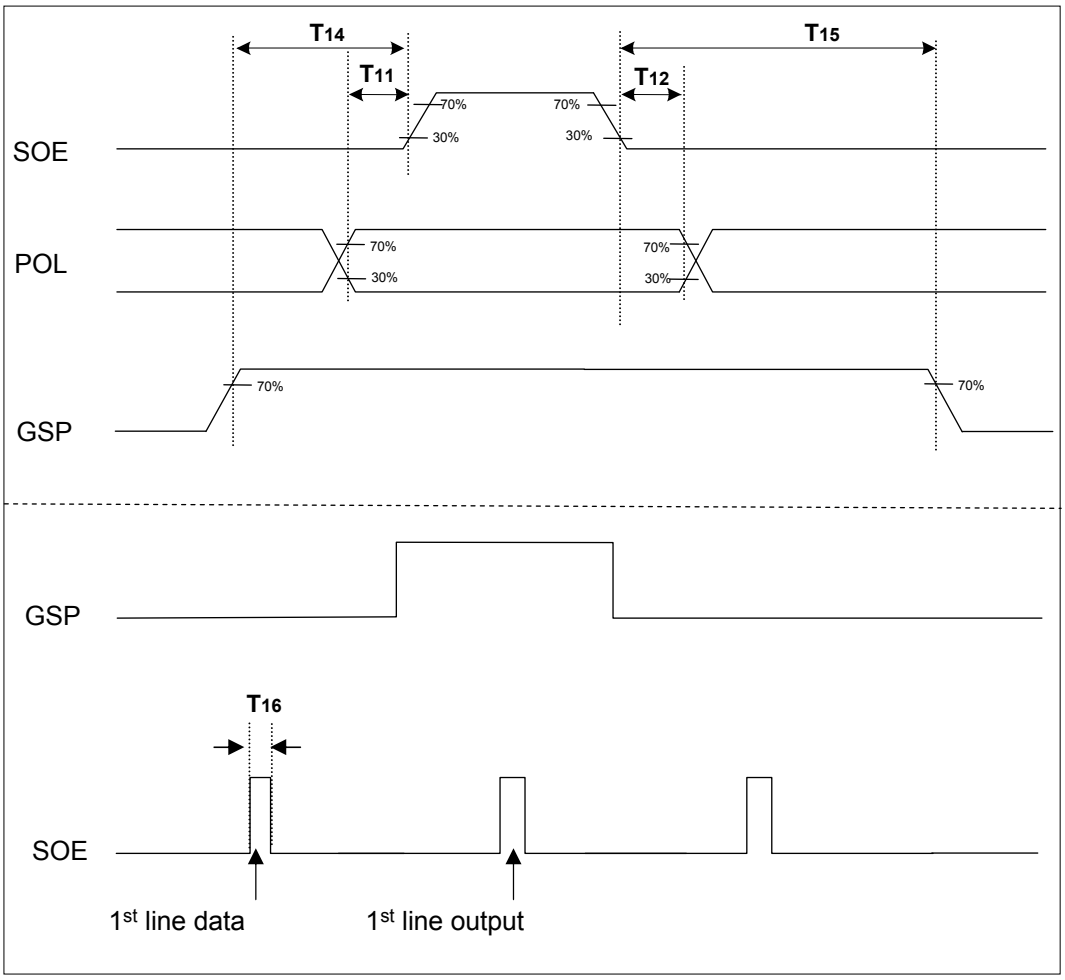
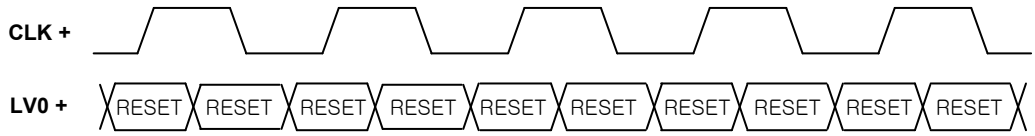


FIG 6. POL, GSP and SOE Timing Waveform

3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV5**.

3-4-1. Control signal input mode



3-4-2. Display data input mode

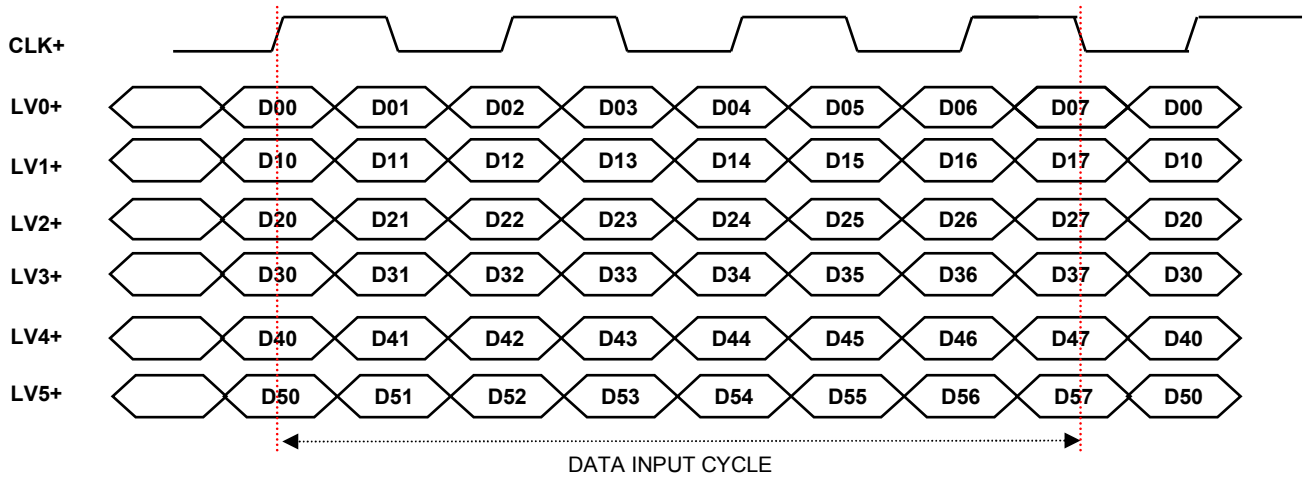


Fig. 7 Mini-LVDS Data

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

3-5. Panel Pixel Structure

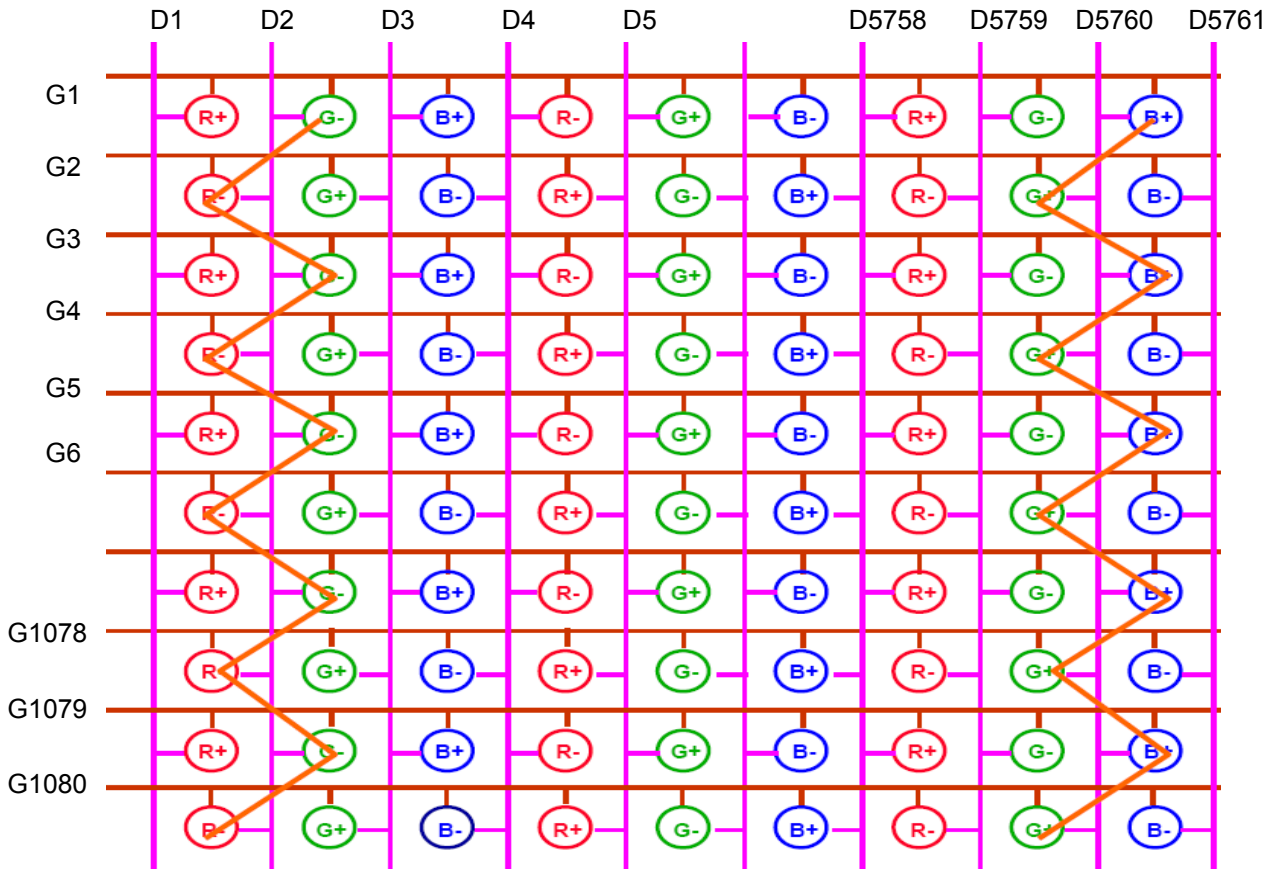


FIG. 8 Panel Pixel Structure

3-6. Power Sequence

3-6-1. LCD Driving circuit

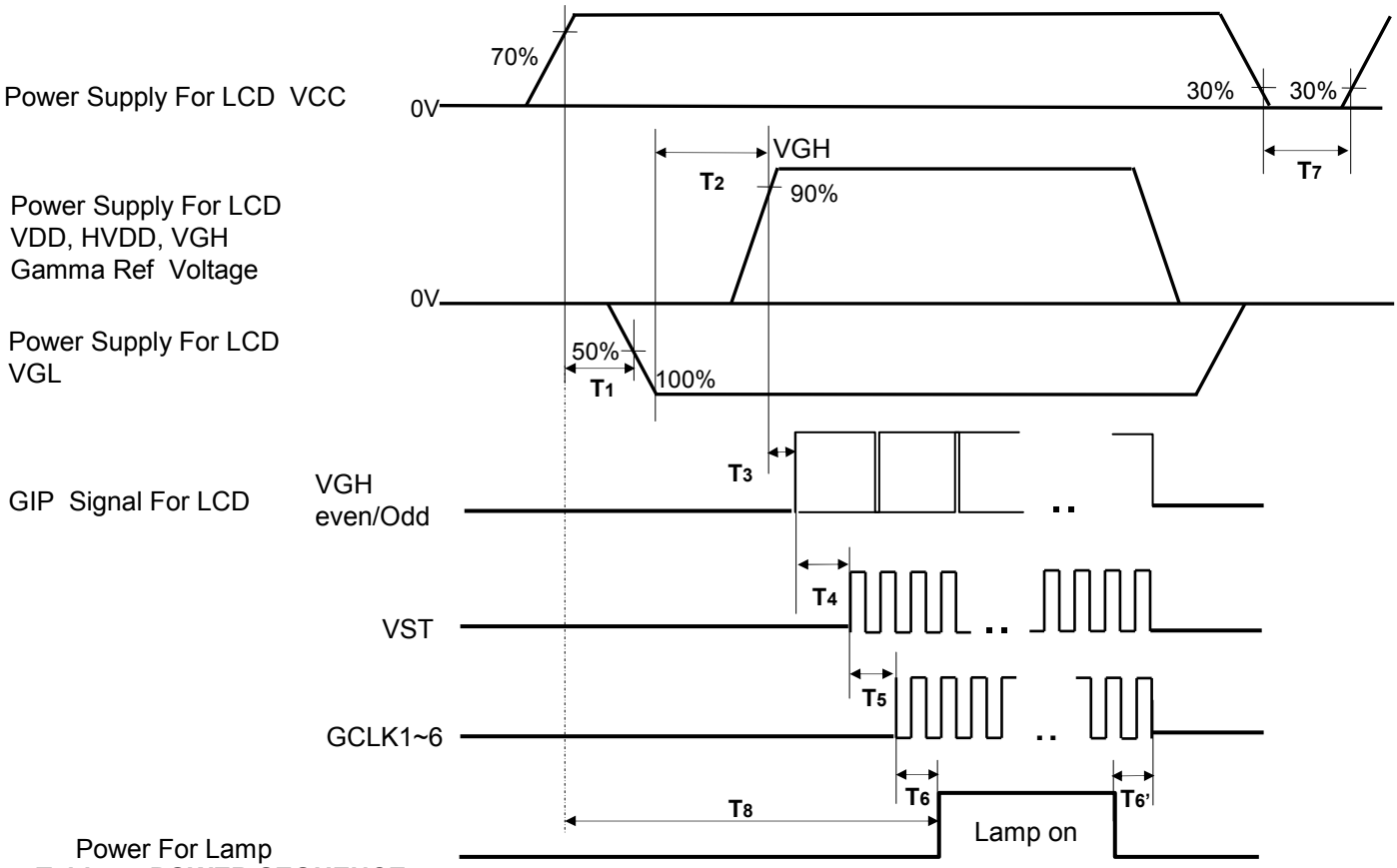
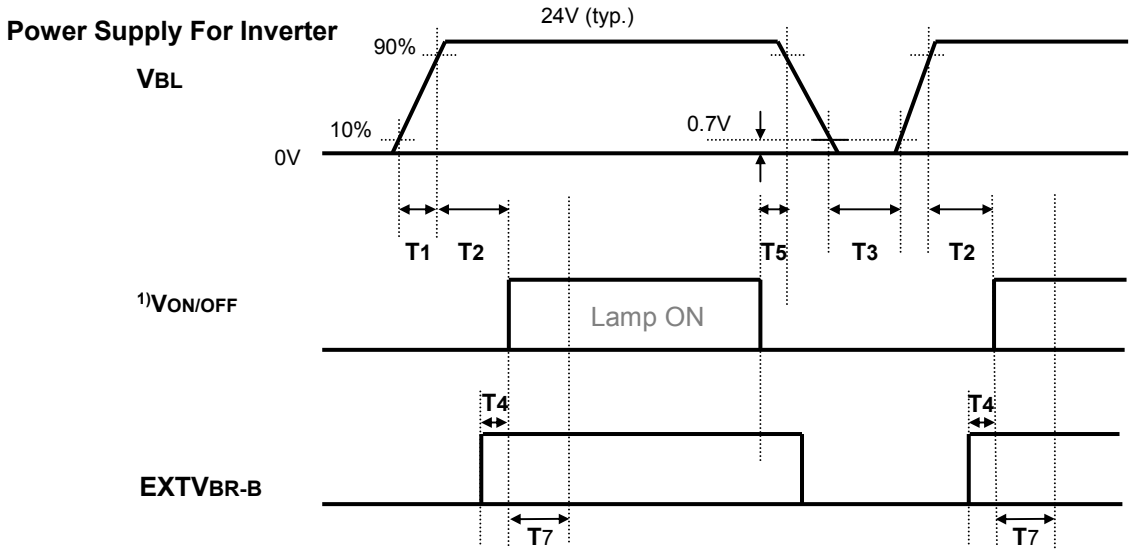


Table 7. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5		-	ms	
T2	0.5		-	ms	
T3	0		-	ms	
T4	10		-	ms	2
T5	0		-	ms	
T6 / T6'	20		-	ms	
T7	2		-	s	
T8	-		12	s	

Note : 1. Power sequence for Source D-IC must be kept. ※ Please refer to Appendix IV-1 for more details.
2. VGH Odd signal should be started “High” status and VGH even & odd can not be “High at the same time.
3. Power Off Sequence order is reverse of Power On Condition including Source D-IC.
4. GCLK On/Off Sequence : GCLK4 → GCLK5 →GCLK6 →GCLK1 → GCLK2 → GCLK3.

3-6-2. Sequence for Inverter



3-6-3. Dip condition for Inverter

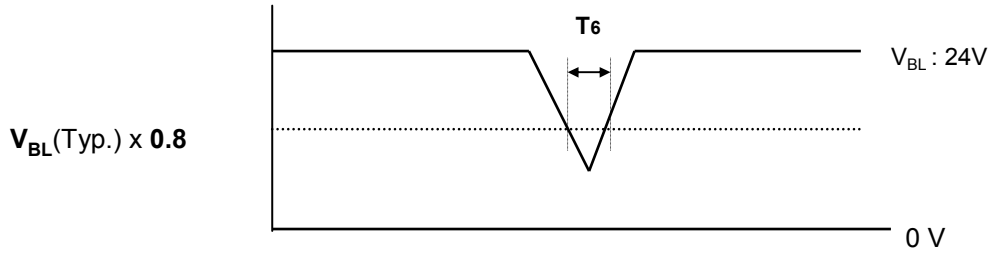


Table 8. Power Sequence for Inverter

Parameter	Values			Units	Note
	Min	Typ	Max		
T1	20	-	-	ms	1
T2	500	-	-	ms	
T3	200	-	-	ms	
T4	0		-	ms	2
T5	10	-	-	ms	
T6	-	-	10	ms	V_{BL}(Typ) x **0.8**
T7	1000	-	-	ms	3

Note : 1. Power sequence for Source D-IC must be kept. ※ Please refer to Appendix IV-1 for more details.
2. VGH Odd signal should be started “High” status and VGH even & odd can not be “High at the same time.
3. Power Off Sequence order is reverse of Power On Condition including Source D-IC.
4. GCLK On/Off Sequence : GCLK4 → GCLK5 →GCLK6 →GCLK1 → GCLK2 → GCLK3.
5, VDD Odd/Even transition time should be within V blank.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.
It is presented additional information concerning the measurement equipment and method in FIG. 9.

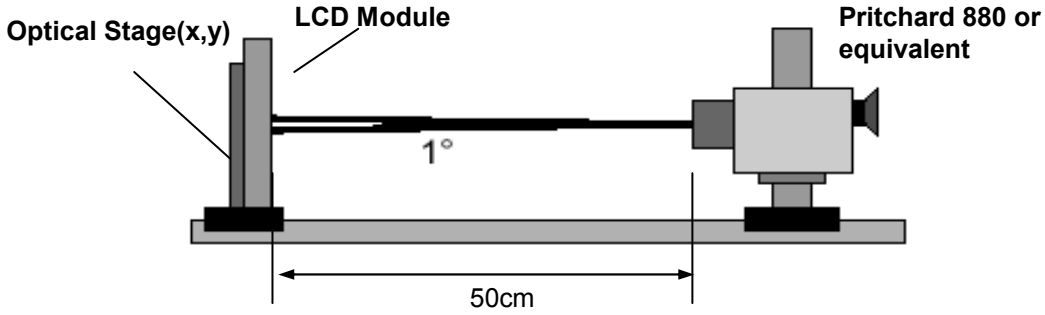


FIG. 9 Optical Characteristic Measurement Equipment and Method

Ta= 25±2°C, VDD,H_VDD,VGH,VGL=typ,
fV=120Hz, Clk=297MHz, IBL=136 mARMS , I out duty = 100%

Table 9. OPTICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	1000	1400	-		1
Surface Luminance, white		L_{WH}	400	500	-	cd/m^2	2
Luminance Variation		δ_{WHITE} 5P	-	-	1.3		3
Response Time	Rising	Tr	-	8	12	ms	4
	Falling	Tf	-	10	14		
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.636	Typ +0.03		
		Ry		0.335			
	GREEN	Gx		0.291			
		Gy		0.603			
	BLUE	Bx		0.146			
		By		0.061			
	WHITE	Wx		0.279			
		Wy		0.292			
Color Temperature				10,000		K	
Color Gamut				72		%	
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	5
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale			-	-	-		6

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at all white pixels}}{\text{Surface Luminance at all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at 25±2°C. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 10.

3. The variation in surface luminance , δ WHITE is defined as :
δ WHITE(5P) = Maximum(L_{on1},L_{on2}, L_{on3}, L_{on4}, L_{on5}) / Minimum(L_{on1},L_{on2}, L_{on3}, L_{on4}, L_{on5})
Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations .
For more information, see the FIG. 10.

4. Response time is the time required for the display to transit from G(255) to G(0) (Rise Time, Tr_R) and from G(0) to G(255) (Decay Time, Tr_D).

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.

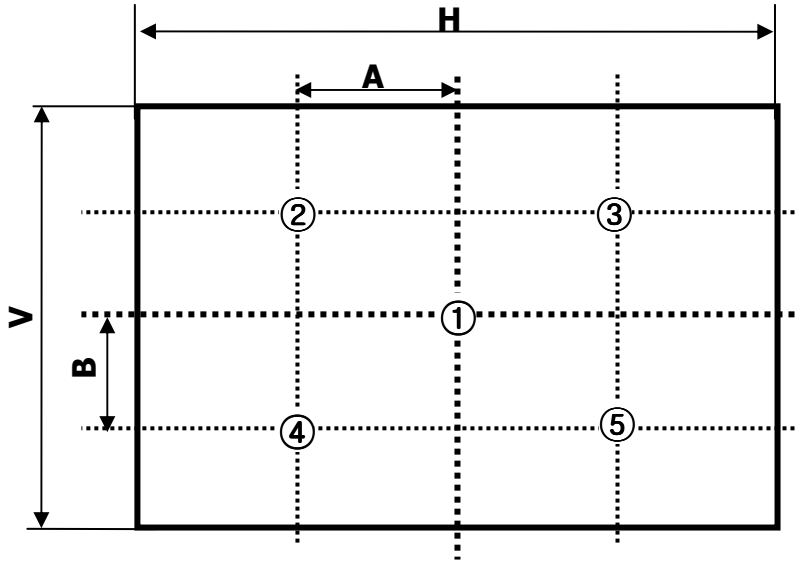
6. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 10.

Table 10. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%]		
	Min.	Typ.	Max.
L0	0.04	0.07	0.14
L63	0.10	0.25	0.42
L127	0.56	1.08	1.64
L191	1.57	2.07	3.63
L255	3.00	4.51	6.80
L319	5.00	7.75	11.2
L383	7.90	12.05	16.3
L447	10.6	17.06	22.8
L511	13.9	22.36	29.3
L575	18.5	28.21	37.5
L639	24.5	35.56	46.3
L703	32.7	43.96	55.1
L767	42.4	53.00	64.2
L831	53.2	63.37	75.0
L895	64.3	74.66	86.3
L959	76.5	86.17	95.0
L1023	100	100	100

	Gray Level	Gamma Ref.
Positive Voltage	L0	Gamma9
	L1	Gamma8
	L31	Gamma7
	L63	Gamma6
	L127	Gamma5
	L191	Gamma4
	L223	Gamma3
	L255	Gamma1
Negative Voltage	L255	Gamma18
	L223	Gamma16
	L191	Gamma15
	L127	Gamma14
	L63	Gamma13
	L31	Gamma12
	L1	Gamma11
	L0	Gamma10

Measuring point for surface luminance & luminance variation



A : H / 4 mm
B : V / 4 mm
@ H,V : Active Area

FIG. 10 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

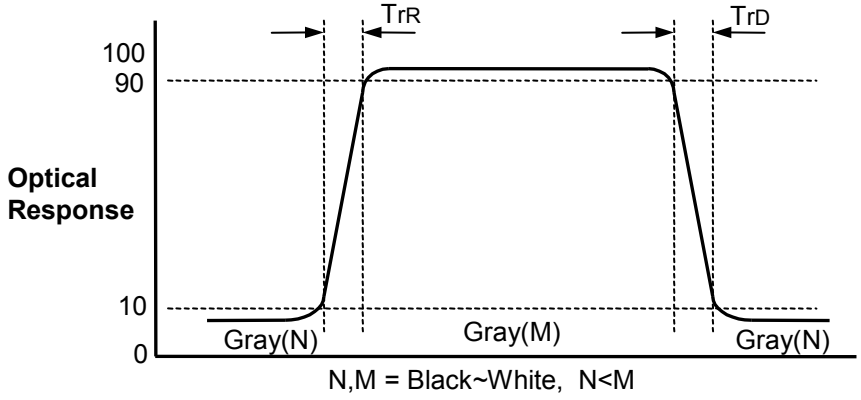


FIG. 11 Response Time

Dimension of viewing angle range

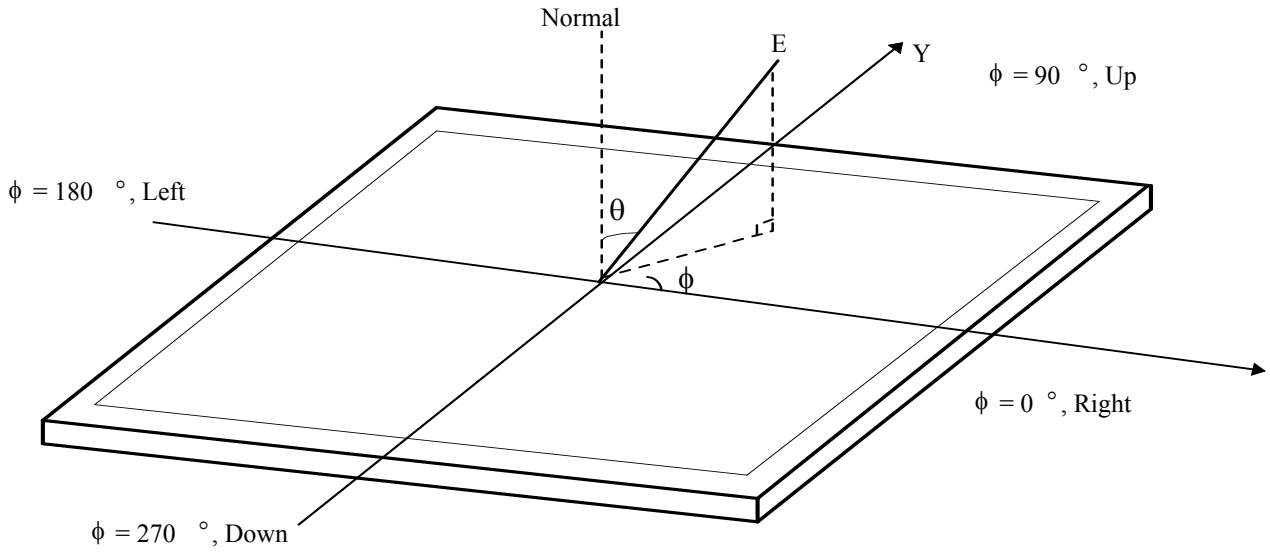


FIG.12 Viewing Angle

5. Mechanical Characteristics

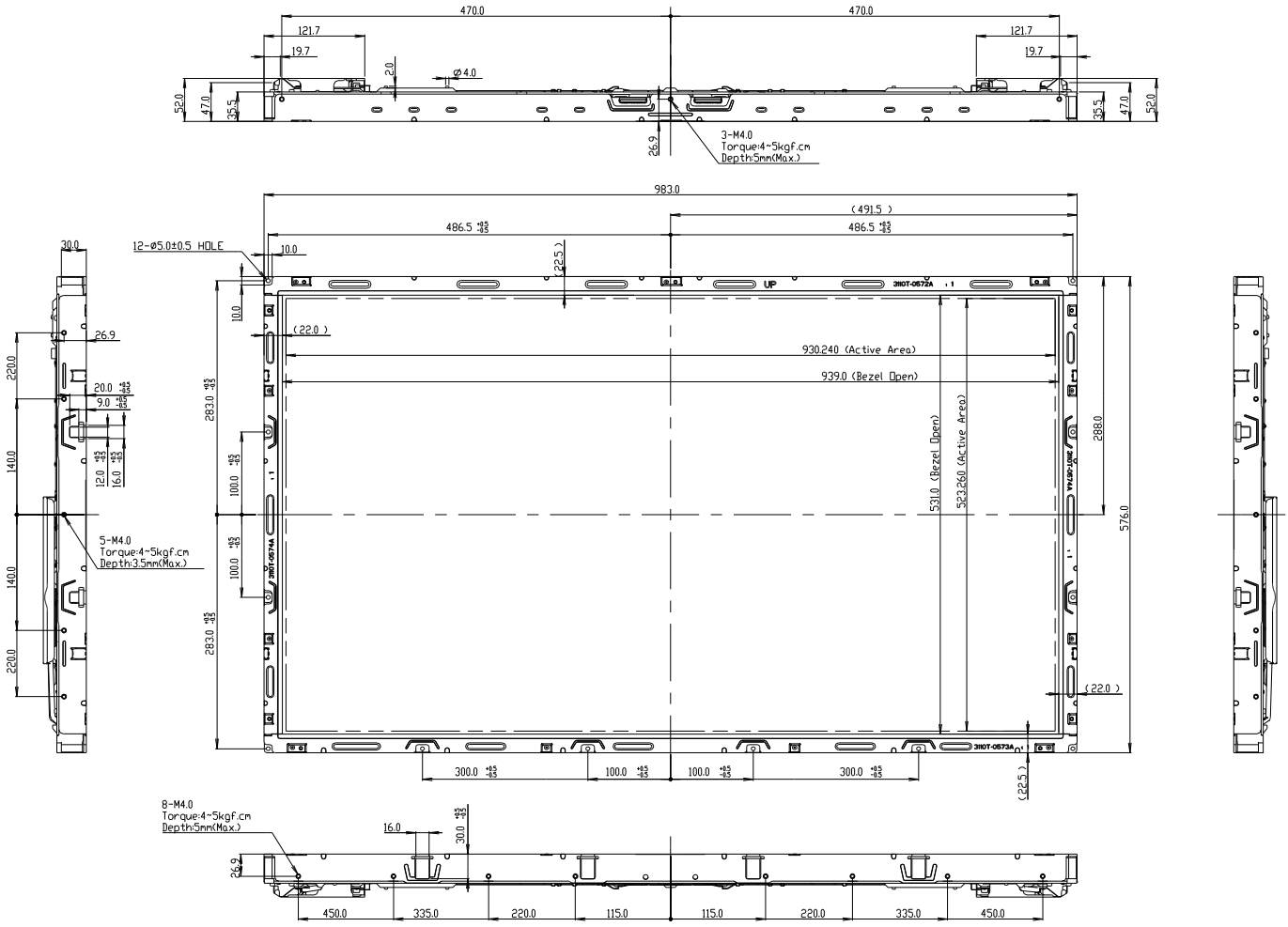
Table 11 provides general mechanical characteristics.

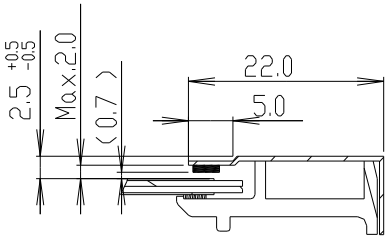
Table 11. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension	Horizontal	983.0 mm
	Vertical	576.0 mm
	Depth	52.0 mm
Bezel Area	Horizontal	939.0 mm
	Vertical	531.0 mm
Active Display Area	Horizontal	930.24 mm
	Vertical	523.26 mm
Weight	9.1 Kg (Typ.) , 10 Kg (Max.)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

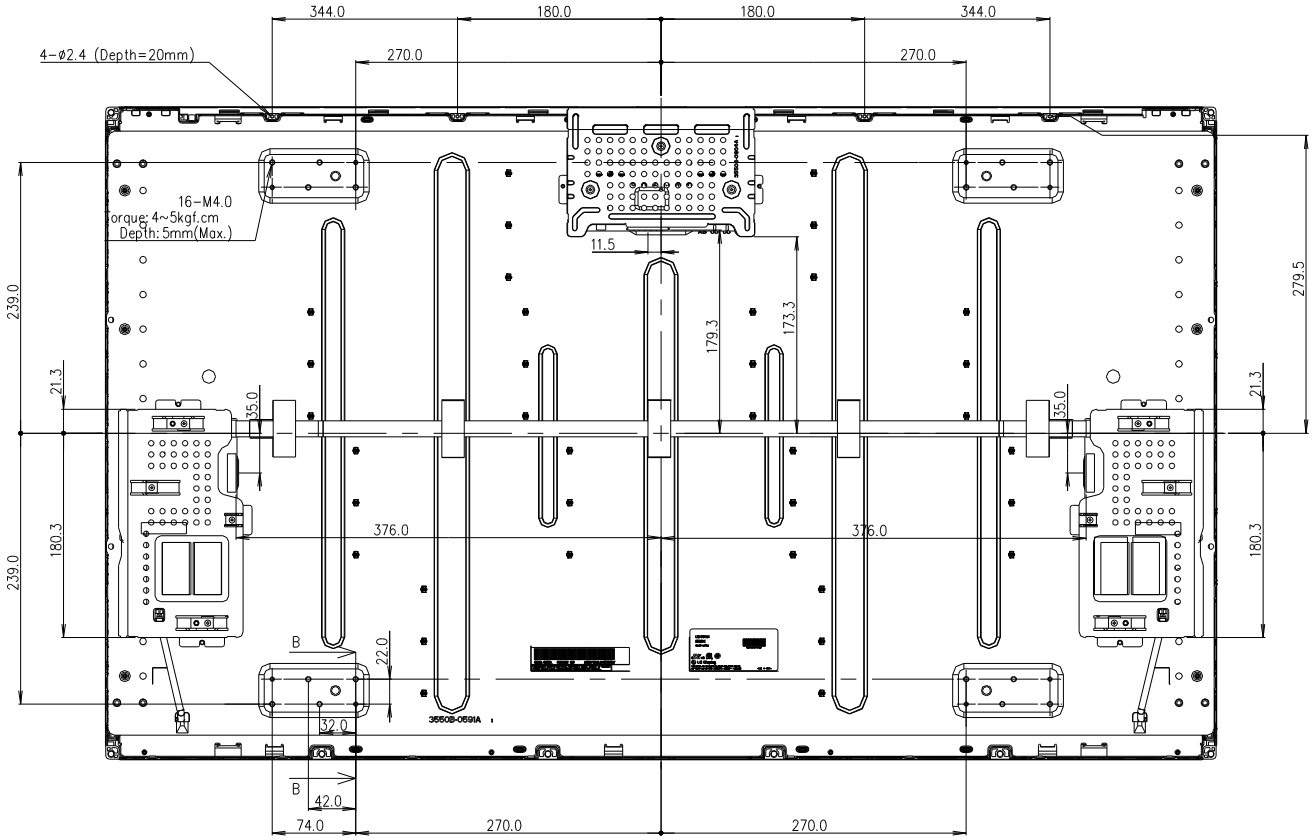
[FRONT VIEW]

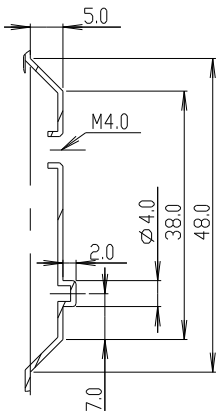




SECTION A-A
SCALE 1/1

[REAR VIEW]





SECTION B-B
SCALE 1/1

6. Reliability

Table 13. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C, 500h
2	Low temperature storage test	Ta= -20°C, 500h
3	High temperature operation test	Ta= 50°C, 80%RH, 500h Ta= 60°C, 500h(2000h)
4	Low temperature operation test	Ta= 0°C, 500h(1000h)
5	Heat cycle test	Ta= -20 °C ~ 60 °C, 30min/5min/30min, 100cycles
6	Soldering heat cycle test	Ta= -40 °C ~ 80 °C, 30min/5min/30min, 200cycles
7	Vibration test (non-operating)	Wave form : random Vibration level : 1.0Grms Bandwidth : 10-300Hz Duration : X,Y,Z Each direction per 10 min.
8	Shock test (non-operating)	Shock level : 50Grms Waveform : half sine wave, 11ms Direction : ±X, ±Y, ±Z One time each direction
9	ESD test	Condition : 150pF, 330 ohm Case , air Evaluation : ± 15kV
10	Humidity storage test	Ta= 40 °C, 70%RH, 240h

Note : Before and after Reliability test, LCM should be operated with normal function.

7. International Standards

7-1. Safety

a) UL 60065, Seventh Edition, Underwriters Laboratories Inc.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

b) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

c) EN 60065:2002 + A11:2008, European Committee for Electrotechnical Standardization (CENELEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

d) IEC 60065:2005 + A1:2005, The International Electrotechnical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

7-2. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Packing

8-1. Information of LCM Label

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	4	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one Pallet : 12 pcs

b) Pallet Size : 1150 mm X 1020 mm X 815 mm.

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9-1. Mounting Precautions

(1) You must mount a module using specified mounting holes (Details refer to the drawings).
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(4) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
(8) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal LCM a fatal blow)
(9) Please do not set LCD on its edge.
(10) The conductive material and signal cables are kept away from transformers to prevent abnormal display, sound noise and temperature rising.
(11) Partial darkness may happen during 3~5 minutes when LCM is operated initially in condition that luminance is under 40% at low temperature (under 5℃). This phenomenon which disappears naturally after 3~5 minutes is not a problem about reliability but LCD characteristic.

(12) Partial darkness may happen under the long-term operation of any dimming without power on/off. This phenomenon which disappears naturally after 5 minutes is not a problem about reliability but LCD characteristics.

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

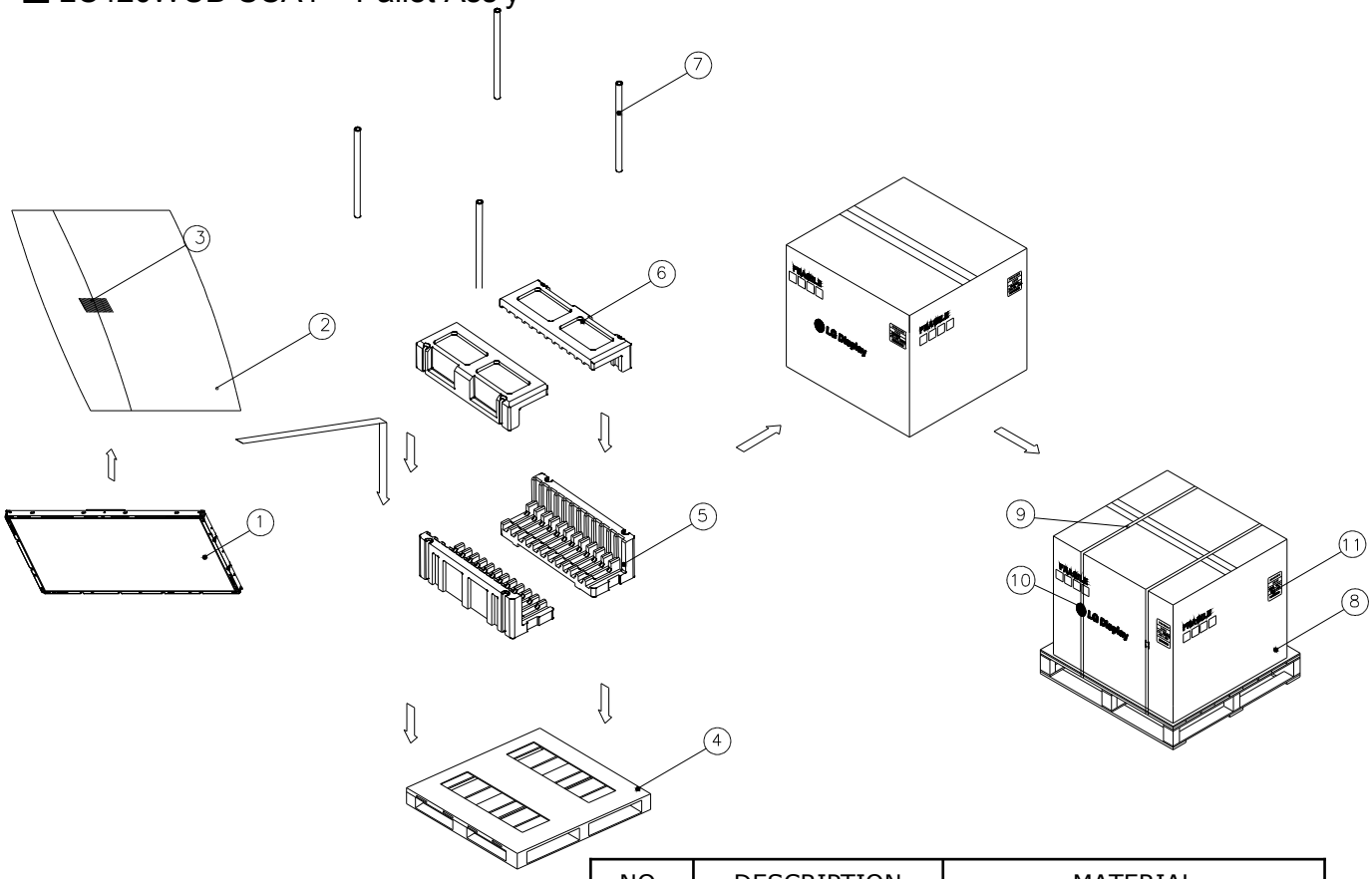
(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX-I

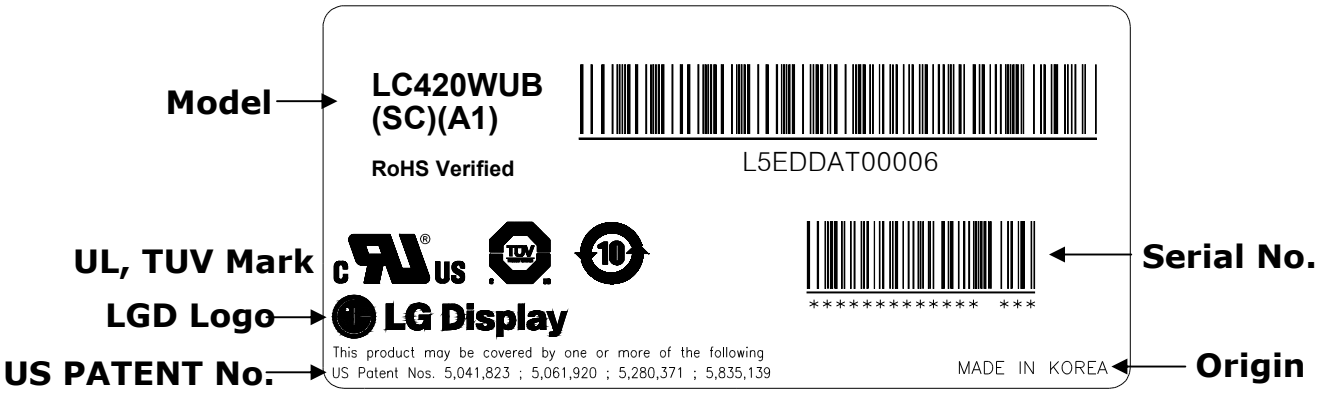
■ LC420WUB-SCA1 – Pallet Ass'y



NO.	DESCRIPTION	MATERIAL
1	LCD Module	
2	BAG	42INCH
3	TAPE	MASKING 20MM X 50M
4	PALLET	Plywood (1140X990X125.5)
5	PACKING	EPS
6	PACKING	EPS
7	ANGLE PACKING	PAPER
8	ANGLE COVER	PAPER
9	BAND,CLIP	STEEL
10	BAND	PP
11	LABEL	YUPO PAPER 80G 100X100

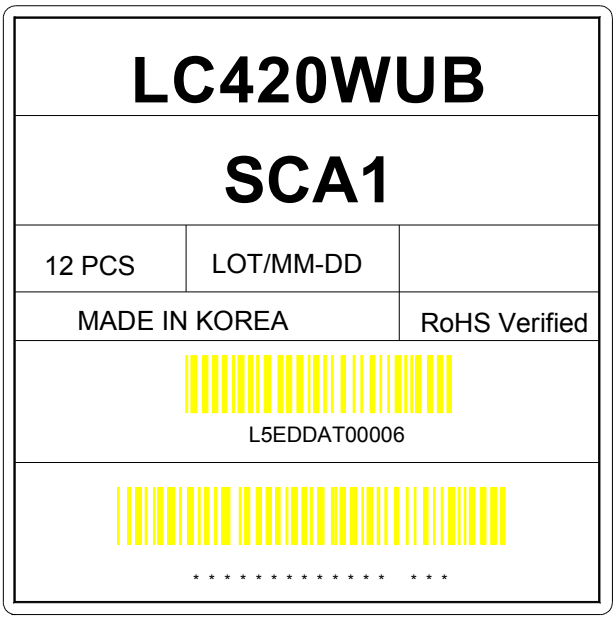
 # APPENDIX- II-1

■ LC420WUB-SCA1-LCM Label



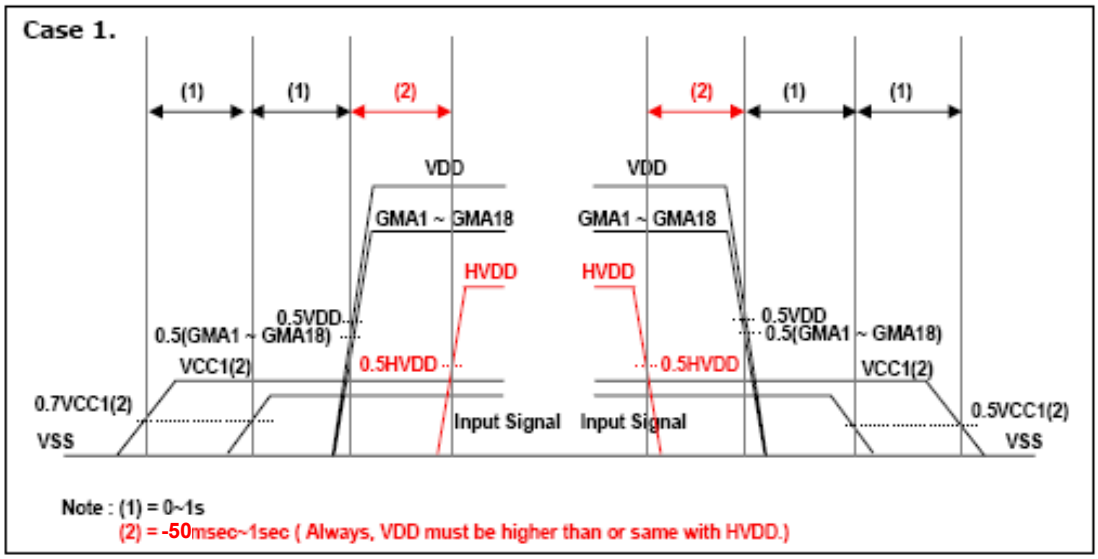
 # APPENDIX- II-2

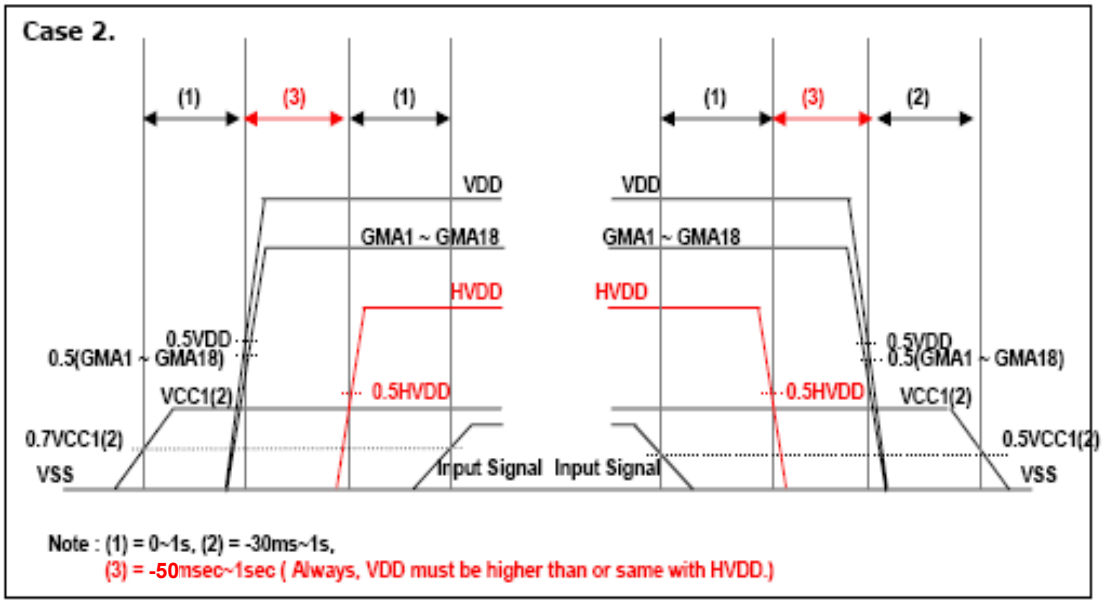
■ LC420WUB-SCA1-Pallet Label



APPENDIX- III

■ LC420WUB-SCA1-Source D-IC Power Sequence





-. Input signal (Input Signal : SOE,POL,GSP, H_CONV, OPT_N)

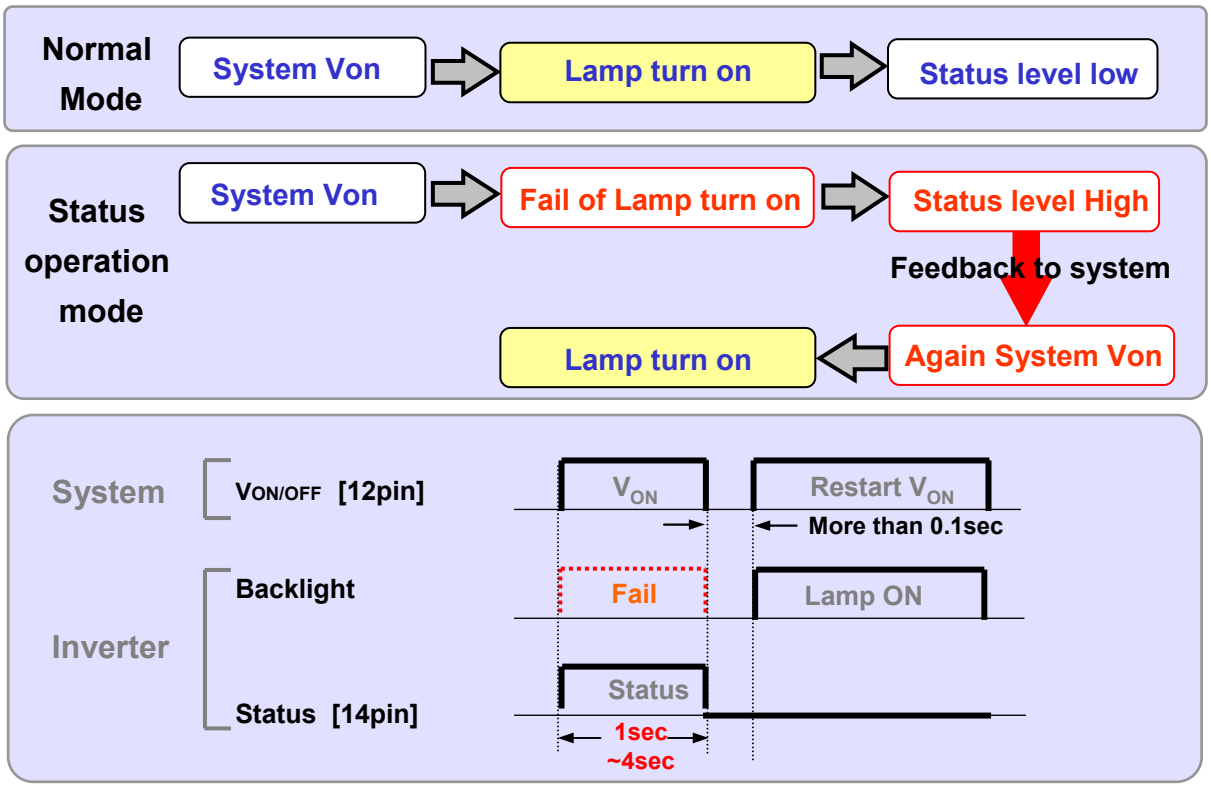
APPENDIX- IV

■ Inverter 14th Pin **(Status)** Design Guide

1) Function of Status pin

- Purpose : Preventing of backlight off by restarting the inverter technically
- How to : When inverter is abnormal operation, TV system inputs the Von signal in the inverter once more to turn on the lamp safely
- Attention : Restart system's Von signal when status pin is high for some time (min:1sec , max:4sec). (The turn on time of lamp can be late such as the low temperature or the storage time)

2) Status operation modes in TV set



3) Inverter pin map

Pin No	Symbol	Description	Inv.
11	NC	No Connection	NC
12	VON/OFF	Backlight ON/OFF control	On/Off
13	**EXTVBR-B**	Burst Dimming Control PWM signal input	External PWM
14	Status	**Normal : Under 0.7V / Abnormal : Upper 3.0V**	**status**